## Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1, 2, 12, 16-18, 20, 24, 25 and 30 have been amended. No claims have been cancelled. Therefore, claims 1-33 are presented for examination.

Claims 30-33 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants submit that claim 30 has been amended to appear in proper condition for allowance.

Applicants acknowledge the allowance of claims 27-29, and that claims 31-33 would be allowable if rewritten.

Claims 1-26 and 30 stand rejected under 35 U.S.C. §102(b) as being anticipated by Jinbo (U.S. Patent No. 5,305,273). Applicants submit that the present claims are patentable over Jinbo.

Jinbo discloses a semiconductor memory device. The device is a non-volatile memory device that includes a memory array 10 connected to an input terminal SIN1 of a sensing circuit 14 via a column selection circuit 12 consisting of N-channel type MOS FETs MY1 to MYn. The sensing circuit 14 has its input terminal SIN1 connected with both the source of an N-channel type MOS FET MN11 and the input of the inverter circuit INV11, and the output VO1 of the inverter circuit INV11 is connected with the gate of the above N-channel type MOS FET MN11. A P-channel type MOS FET MP11 serving as a load MOS FET has its source connected with the power supply VC and its gate and drain connected with the drain of the N-channel type MOS FET MN11. From the contact N1OO where the gate and drain of the P-channel type MOS FET MP11 and the drain of the N-channel type MOS FET MN11 are connected, the output Vsal of the sensing circuit 14 is output.

A reference voltage generation circuit 15 has a configuration similar to the sensing circuit 14; it comprises an N-channel type MOS FET MN12, an inverter circuit INV12 and a P-channel type MOS FET MP12. Input is provided to a reference memory device MCR1 equivalent to the

memory devices MCll to MCmn via an N-channel type MOS FET MYR1 equivalent to the N-channel type MOS FETs MYl to MYn constituting the column selection circuit 12. The reference voltage generation circuit 15 generates reference voltage Vral. A comparison amplifier 16 compares the output Vsal from the sensing circuit 14 with the output Vral from the reference voltage generation circuit 15 and outputs the result data output DATl. The semiconductor memory device of this embodiment is further provided with an N-channel type MOS FET MN13 between the input SINl of the sensing circuit 14 and the input RINl of the reference voltage generation circuit 15. The gate of this N-channel type MOS FET MN13 is connected with the output VOl of the inverter circuit INVll. See Jinbo at Figure 1 and col. 4, ll. 20 – col. 5, ll. 11.

If the selected memory devices are in non-write status, the input SIN1 of the sensing circuit 14 is discharged by the selected memory device and becomes low level. Low potential at the input SIN1 of the sensing circuit 14 causes the output VO1 of the inverter circuit INV11 to be high level, and the N-channel type MOS FET MN11 to become conductive. Accordingly, the output Vsa1 of the sensing circuit 14 is at low level. At this point, the gate of the N-channel type MOS FET MN13 also becomes high level. However, since the selected memory device and the reference memory device have the same characteristics, the input SIN1 of the sensing circuit 14 and the input RIN1 of the reference voltage generation circuit 15 are at the same (low) voltage level. This results in no current flow via the N-channel type MOS FET MN13. Accordingly, the output Vsa1 of the sensing circuit 14 and the output Vra1 of the reference voltage generation circuit 15 are both at low level.

However, if the selected memory device is in write status, the input SIN1 of the sensing circuit 14 is charged via the P-channel type MOS FET MP11 and the N-channel type MOS FET MN11 and becomes high level. Increase of the potential at the input SIN1 of the sensing circuit 14 causes the output VO1 of the inverter circuit INV11 to be low. This results in that the N-channel type MOS FET MN11 becomes non conductive and the output Vsa1 of the sensing circuit 14 is brought to high level by the P-channel type MOS FET MP11. At this point, the input SIN1 of the sensing circuit 14 has higher voltage than the input RIN1 of the reference

voltage generation circuit 15, but the gate voltage of the N-channel type MOS FET MN13 is at low level and the potential difference between its source and drain is small, which results in little current flow. Therefore, the output Vsa1 of the sensing circuit 14 is at high level and the output Vra1 of the reference voltage generation circuit 15 is at low level. The comparison amplifier 16 compares the potentials at the output Vsa1 of the sensing circuit 14 which changes depending on the status of the selected memory device and the output Vra1 of the reference voltage generation circuit 15 so as to output DAT1 corresponding to the status of the memory device (col. 5, ll. 12 – col. 6, ll. 6).

Claim 1 of the present application recites a control signal to control operation of an equalization circuit by causing the equalization circuit to equalize a first input and a second input of a sense amplifier prior to changes induced by a first drain bias network and a second bias network. Applicants submit that Jinbo does not disclose equalizing a first input and a second input of a sense amplifier prior to changes induced by a first drain bias network and a second bias network. Jinbo discloses pulling a sensing input and a reference input to the same voltage level whenever a selected memory device has a non-write status. However, such a function is not the same as equalizing a first input and a second input of a sense amplifier prior to changes induced by a first drain bias network and a second bias network. Therefore, claim 1 is patentable over Jinbo.

Claims 2-11 depend from claim 1 and include additional limitations. Therefore, claims 2-11 are also patentable over Jinbo.

Claim 12 recites equalizing a sense input and a reference input using a single equalizing transistor by causing the equalization transistor to equalize a first input and a second input of a sense amplifier prior to changes being induced by. Therefore, for the reasons described above with respect to claim 1, claim 12 is also patentable over Jinbo. Since claims 13-15 depend from claim 12 and include additional limitations, claims 13-15 are also patentable over Jinbo.

Claim 16 recites a single equalizing transistor having a first node and a second node, the equalizing transistor coupled to the input of the first bias means and coupled to the input of the

second bias means, the equalizing transistor to equalize a first input and a second input of the comparison means prior to changes induced by the first bias means and the second bias means. Thus, for the reasons described above with respect to claim 1, claim 16 is also patentable over Jinbo. Since claims 17-19 depend from claim 16 and include additional limitations, claims 17-19 are also patentable over Jinbo.

Claim 20 recites a control signal to control operation of a equalization circuit, to cause the equalization circuit to equalize a first input and a second input of the comparison circuit prior to changes induced by a first drain bias network and a second bias network. Accordingly, for the reasons described above with respect to claim 1, claim 20 is also patentable over Jinbo. Since claims 21-23 depend from claim 20 and include additional limitations, claims 21-23 are also patentable over Jinbo.

Claim 24 recites a control signal to control operation of an equalization circuit by causing the equalization circuit to equalize a first input and a second input of a comparison circuit prior to changes induced by a first drain bias network and a second bias network. Thus, for the reasons described above with respect to claim 1, claim 24 is also patentable over Jinbo. Since claims 25 and 26 depend from claim 24 and include additional limitations, claims 25 and 26 are also patentable over Jinbo.

Claim 30 recites a control signal to control operation of an equalization circuit by causing the equalization circuit to equalize a first input and a second input of a comparison circuit prior to changes induced by a first drain bias network and a second bias network. For the reasons described above with respect to claim 1, claim 30 is also patentable over Jinbo. Since claims 31-33 depend from claim 30 and include additional limitations, claims 31-33 are also patentable over Jinbo.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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**Versions with Markings to Show Changes Made**
**Insertions are underlined; deletions are bracketed.**

1. (Twice Amended) An apparatus comprising:

a first drain bias network having an input suitable to couple to a FLASH cell;

a second drain bias network having an input suitable to couple to a FLASH cell; and

a sense amplifier having a first input, a second input, and an output;

an equalization circuit having a first node coupled to the input of the first drain bias network and having a second node coupled to the input of the second drain bias network and having a control signal to control operation of the equalization circuit[, wherein the equalization circuit is a single equalization transistor coupled between the first drain bias network and the second drain bias network.] by causing the equalization circuit to equalize the first input and the second input of the sense amplifier prior to changes induced by the first drain bias network and the second bias network.

2. (Amended) The apparatus of claim 1[ further comprising:

a sense amplifier having a first input, a second input, and an output; and] wherein[:] the first drain bias network has an output coupled to the first input of the sense amplifier and the second drain bias network has an output coupled to the second input of the sense amplifier.

12. (Twice Amended) A method comprising:

equalizing a sense input and a reference input using a single equalizing transistor by causing the equalization transistor to equalize a first input and a second input of a sense amplifier prior to changes being induced by;

coupling the sense input to a FLASH cell to be sensed;

terminating equalization of the sense input and the reference input; and

measuring a sense voltage, the sense voltage corresponding to the sense input.

16. (Twice Amended) An apparatus comprising:

a first bias means for biasing a FLASH cell, the first bias means having an input and an output;

a second bias means for biasing a reference FLASH cell, the second bias means having an input and an output; and

a comparison means for comparing the output of the first bias means and the output of the second bias means;

a single equalizing transistor having a first node and a second node, the equalizing transistor coupled to the input of the first bias means and coupled to the input of the second bias means, the equalizing transistor to equalize a first input and a second input of the comparison means prior to changes induced by the first bias means and the second bias means.

17. (Amended) The apparatus of claim 16 further comprising:

[a comparison means for comparing the output of the first bias means and the output of the second bias means.]

a FLASH cell selectively coupled to the input of the first bias means.

18. (Amended) The apparatus of claim 17 further comprising:

[a FLASH cell selectively coupled to the input of the first bias means; and]

a reference FLASH cell coupled to the input of the second bias means.

20. (Twice Amended) A FLASH device comprising:

a FLASH cell array;

a control circuit block coupled to the FLASH cell array to control the FLASH cell array; and

a comparison circuit block coupled to the FLASH cell array and coupled to the control circuit block, the control circuit block to control the comparison circuit, the comparison circuit including:

a first drain bias network having an input suitable to couple to a FLASH cell,

a second drain bias network having an input suitable to couple to a FLASH cell, and

an equalization circuit having a first node coupled to the input of the first drain bias network and having a second node coupled to the input of the second drain bias network and having a control signal to control operation of the equalization circuit, [wherein the equalization circuit is a single equalizing transistor coupled between the first drain bias network and the second drain bias network] to cause the equalization circuit to equalize the first input and the second input of the comparison circuit prior to changes induced by the first drain bias network and the second bias network.

24. (Amended) An apparatus comprising:

a first bias network having an input suitable to couple to a persistent memory storage location;

a second bias network having an input suitable to couple to a persistent memory storage location; and

a sense amplifier having a first input, a second input, and an output;

an equalization circuit having a first node coupled to the input of the first bias network and having a second node coupled to the input of the second bias network and having a control signal to control operation of the equalization circuit[, wherein the equalization circuit is a single equalizing transistor coupled between the first drain bias network and the second drain bias network] by causing the equalization circuit to equalize the first input and the second input of the comparison circuit prior to changes induced by the first drain bias network and the second bias network.

25. (Amended) The apparatus of claim 24[ further comprising:

a sense amplifier having a first input, a second input, and an output; and] wherein[:] the first bias network has an output coupled to the first input of the sense amplifier and the second bias network has an output coupled to the second input of the sense amplifier, the output of the first bias network having a relationship with the input of the first bias network, the output of the second bias network having a relationship with the input of the second bias network.

30. (Amended) An apparatus comprising:

a reference cell;

a kicker circuit;

a reference kicker circuit coupled to an output of the reference cell;

a first drain bias network coupled to the kicker circuit;

a second drain bias network coupled to the reference kicker circuit;

a sense amplifier with a first input to coupled to an output of the first drain bias network and the sense amplifier with a second input coupled to an output of the second drain bias network; and

an equalizing transistor, coupled between an input of the kicker circuit and an input of the reference kicker circuit, having a control signal to control operation of the equalization circuit by causing the equalization circuit to equalize the first input and the second input of the sense amplifier prior to changes induced by the first drain bias network and the second bias network.